PCA9521

Fast dual bidirectional bus buffer

Rev. 1 — 22 August 2011 Product data sheet

1. General description

The PCA9521 is a monolithic bipolar integrated circuit for bus buffering in applications including I^{2}C-bus, SMBus, PMBus, and other systems based on similar principles.

The buffer extends the bus load limit by buffering both the SCL and SDA lines. It supports up to 400 pF loads on each side of the buffer at 400 kHz. Higher capacitance is supported at lower speeds, and lower capacitance at higher speeds up to 1 MHz.

The enable function allows sections of the bus to be isolated. Individual parts of the system can be brought on-line successively. This means a controlled start-up using a diverse range of components, operating speeds and loads is easily achieved. Systems employing removable components on a back-plane (e.g., telecommunications racks) can use the enable pin and the high-impedance ports on power-down to safely install and remove components in active systems.

Bus level translation between a very wide range of bus voltages, from 1.8 V to 10 V, is supported. This feature provides enormous flexibility in interfacing systems of different technologies.

The unique operation of the PCA9521 provides one of the fastest response times of such bidirectional buffers, ensuring any glitches (common to other buffers) are kept well within the 50 ns I^{2}C-bus specification. Additionally, it does this without the need for ‘rise-time accelerators’ which, combined with low noise margins, may cause glitches outside of the I^{2}C-bus specification.

2. Features and benefits

- Dual, bidirectional unity gain buffer
- Fast switching times allow operation in excess of 1 MHz
- Supports I^{2}C-bus (Standard-mode and Fast-mode), SMBus (standard and high power mode), PMBus and IPMB
- Enable allows bus segments to be disconnected
- Low standby current when not enabled
- Application/removal of power to IC will not interfere with other bus activity
- 6 mA (static) pull-down capability supports a wide range of bus standards
- Low noise susceptibility
- Low input-output offset voltage
- Threshold and offset parameters allow the connection of several devices in series
- Bus levels independent of supply voltage
- Operating voltages from 2.7 V to 5.5 V
- Wide range of bus voltages from 1.8 V to 10 V

- Level shifting between different bus voltages
- Achieves superior response times without the need for rise time accelerators
- ESD protection exceeds 2 kV HBM per JESD22-A114 and 500 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA

3. Applications

- Power management systems
- Telecommunications systems including ATCA
- Desktop and portable computers including RAID
- Building automation
- TV/projector/monitor interconnection
- Game consoles/boxes
- CompactPCI
- Medical systems
- Gaming machine networks
- Backplane management/interconnect

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9521D	PCA9521	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9521DP	9521	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

5. Block diagram

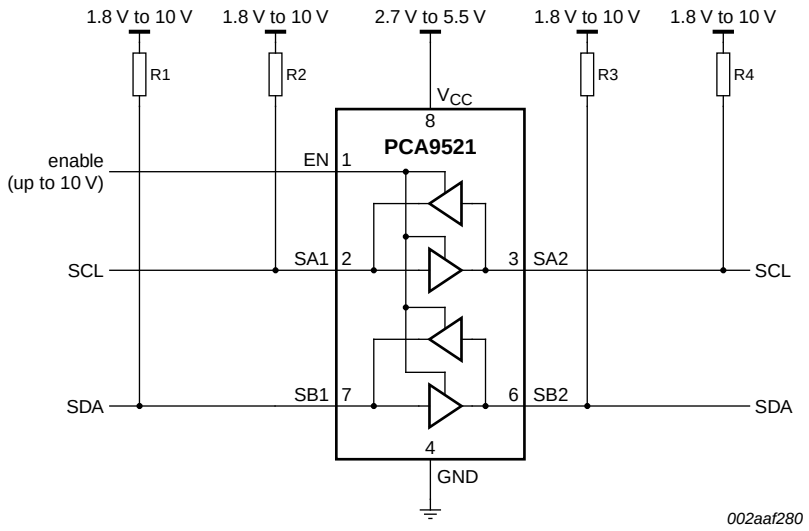


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

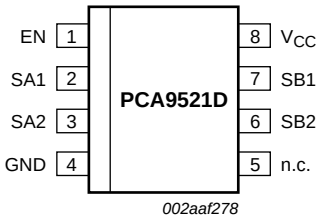


Fig 2. Pin configuration for SO8

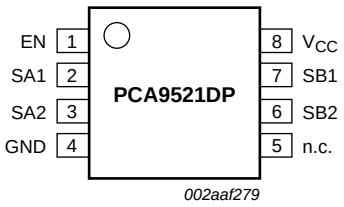


Fig 3. Pin configuration for TSSOP8

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
EN	1	enable
SA1	2	buffer A, port 1 (SCL output[1])
SA2	3	buffer A, port 2 (SCL input[1])
GND	4	supply ground
n.c.	5	not connected
SB2	6	buffer B, port 2 (SDA input[1])
SB1	7	buffer B, port 1 (SDA output[1])
V_{CC}	8	positive supply

[1] Recommended I^2C-bus orientation for device family compatibility.

7. Functional description

Refer to Figure 1 “Block diagram”.

7.1 V_{CC}, GND — supply pins

The power supply voltage for the PCA9521 may be any voltage in the range 2.7 V to 5.5 V. The threshold level below which the output will begin to match the input is 33 % of V_{CC}. Hence, the operating voltage should be chosen with the required bus voltage, switching threshold, and noise margins, in mind.

7.2 SA1, SA2, SB1, SB2 — buffer inputs/outputs

The two buffers (SA and SB) are identical and symmetrical. The buffers can be driven from either direction, with the same response. When port 1 of the buffer is being driven LOW (< $0.3V_{CC}$) by another device on the bus, port 2 will be driven LOW by the IC to provide the buffered output.

The ‘input’ side is determined by the lowest externally driven signal. Therefore if port 1 is externally pulled to V_{Sx1} = 250 mV, and port 2 is externally pulled to V_{Sx2} = 500 mV, the buffer will pull port 2 down further such that it becomes $V_{Sx2} = V_{Sx1} + V_{offset}$. Should port 2 subsequently become lower than port 1 by the amount of the offset voltage ($V_{Sx2} + V_{offset} < V_{Sx1}$) by means of an external device pulling it LOW, control of the buffering operation will switch, and port 2 will become the ‘input’. The voltage at port 1 will then become $V_{Sx1} = V_{Sx2} + V_{offset}$. When both ports are being held almost equal (less than an offset voltage) the external devices are effectively in control.

7.3 EN — enable; activate buffer operations

The enable input, EN, is used to disable the buffer, for the purpose of isolating sections of the bus. The IC should only be disabled when the bus is idle. This prevents truncation of commands which may confuse other devices on the bus.

Enable may also be used to progressively activate sections of the bus during system start-up. Bus sections slow to respond on power-up can be kept isolated from the main system to avoid interference and collisions.

The EN pin may be pulled up higher than the V_{CC} of the buffer, further enhancing the capability of the PCA9521 in a level shifting role. For example, a microprocessor could drive EN, SA1 and SB1 at 5 V, while the buffer V_{CC}, SA2 and SB2 ports are at 3.3 V.

Similarly, the threshold level of the EN pin allows a 1.8 V device to disable an PCA9521 with a V_{CC} of 3.3 V.

The EN pin includes an internal 2 μA pull-down current, which will act to disable the device should the pin be left floating.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage		[1]	−0.3	+7	V
V_n	voltage on any other pin	SA1, SA2, SB1, SB2	[1]	−0.3	+12	V
$V_{I(EN)}$	input voltage on pin EN		[1]	−0.3	+12	V
I_{IO}	input/output current	any pin		-	20	mA
P_{tot}	total power dissipation			-	300	mW
T_{stg}	storage temperature			−55	+125	°C
T_{amb}	ambient temperature	operating		−40	+85	°C

[1] Voltages are specified with respect to pin 4 (GND).

9. Characteristics

Table 4. Characteristics

T_{amb} = −40 °C to +85 °C; voltages are specified with respect to ground (GND).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power supply						
V_{CC}	supply voltage	operating	2.7	-	5.5	V
I_{CC}	supply current	operating; V_{CC} = $V_{I(EN)}$ = 5.5 V	-	9	-	mA
		standby; V_{CC} = 5.5 V; $V_{I(EN)}$ = 0 V	-	295	350	µA
Buffer ports (SA1, SA2, SB1, SB2)						
V_{bus}	bus voltage		-	-	10	V
$V_{th(IL)}$	LOW-level input threshold voltage		-	-	$0.3V_{CC}$	V
$V_{th(IH)}$	HIGH-level input threshold voltage		$0.41V_{CC}$	-	-	V
I_{IL}	LOW-level input current	drive current; V_{bus} < V_{CC}	-	−12	−30	µA
$I_{O(sink)}$	output sink current	LOW-level; $V_{bus(out)}$ = 0.4 V	6	-	-	mA
V_{offset}	offset voltage	input/output; V_{CC} = 3.3 V				
		I_{OL} = 4 mA; $V_{bus(in)}$ = 50 mV	-	165	200	mV
		I_{OL} = 500 µA; $V_{bus(in)}$ = 50 mV	-	55	100	mV
		I_{OL} = 1.2 mA; $V_{bus(in)}$ = 200 mV	-	60	100	mV
I_L	leakage current	$V_{bus} \geq V_{CC}$	-	-	5	µA
C_{io}	input/output capacitance	[1]	-	-	10	pF
Enable (EN)						
V_{en}	enable voltage	active	1.2	-	-	V
V_{dis}	disable voltage	standby	-	-	0.7	V
I_I	input current	V_{en} > 1.2 V	1	-	5	µA

Table 4. Characteristics *...continued*

T_{amb} = −40 °C to +85 °C; voltages are specified with respect to ground (GND).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Timing characteristics[1]						
t_d	delay time	V_{CC} = 5 V; V_{bus} = 5 V; $R_{pu(bus)}$ = 1 kΩ; $C_{L(ext)}$ = 120 pF; Figure 4	-	30	-	ns
t_f	fall time	V_{CC} = 5 V; V_{bus} = 5 V; $R_{pu(bus)}$ = 1 kΩ; $C_{L(ext)}$ = 120 pF; Figure 4	-	15	-	ns
$f_{oper(I2C)}$	I^2C operating frequency		0	-	400	kHz
$f_{oper(max)}$	maximum operating frequency		1000	-	-	kHz
$t_{d(en-act)}$	enable to active delay time	EN HIGH to Sxx active	-	1	-	µs
$t_{d(dis-stb)}$	disable to standby delay time	EN LOW to Sxx disabled	-	1.1	-	µs

[1] Guaranteed by design (not subject to test).

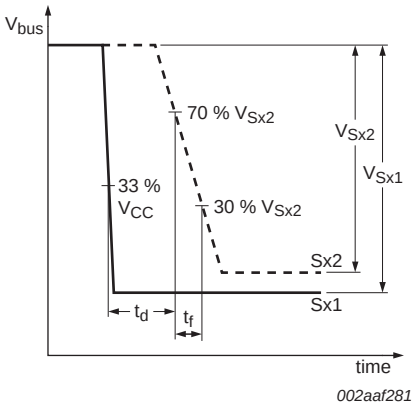
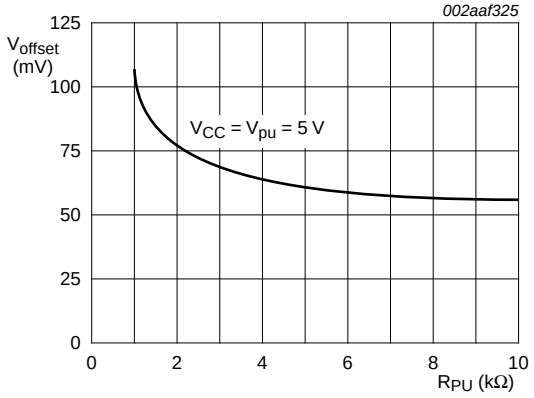


Fig 4. Timing parameters



T_{amb} = 25 °C; $V_{bus(in)}$ = 200 mV.

Fig 5. Offset voltage, $V_O - V_I$

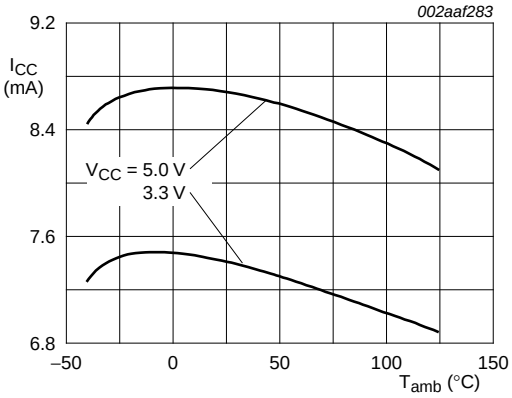
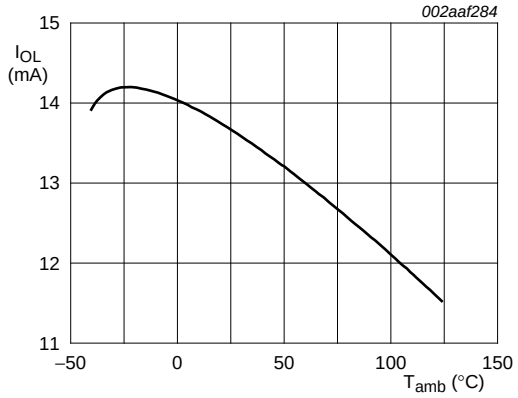
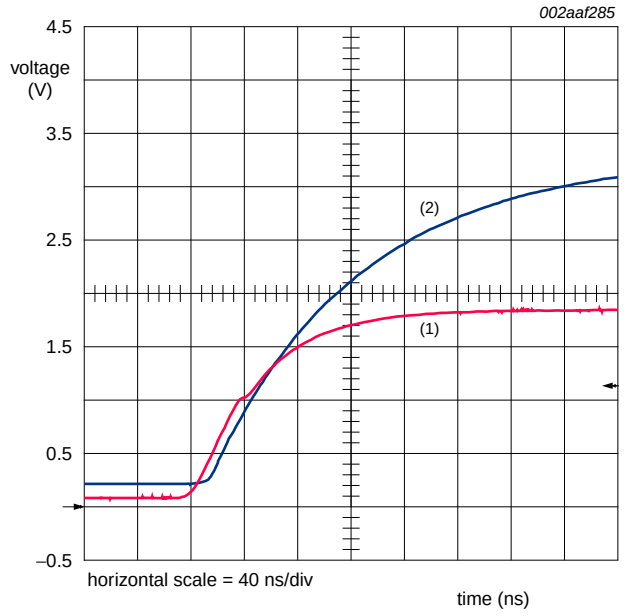


Fig 6. Supply current versus ambient temperature



$V_{bus(out)}$ = 500 mV; V_{CC} = 2.7 V.

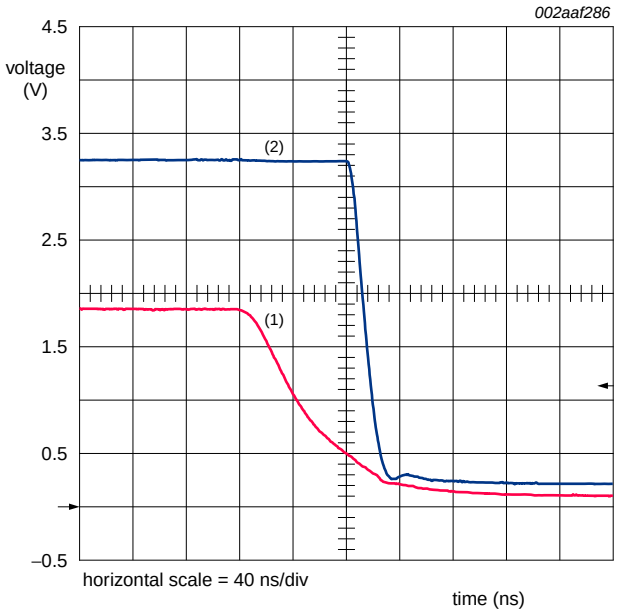
Fig 7. LOW-level output current versus ambient temperature



(1) Input 33 pF

(2) Output 120 pF

Fig 8. Rise time (4 mA pull-up)



(1) Input 33 pF

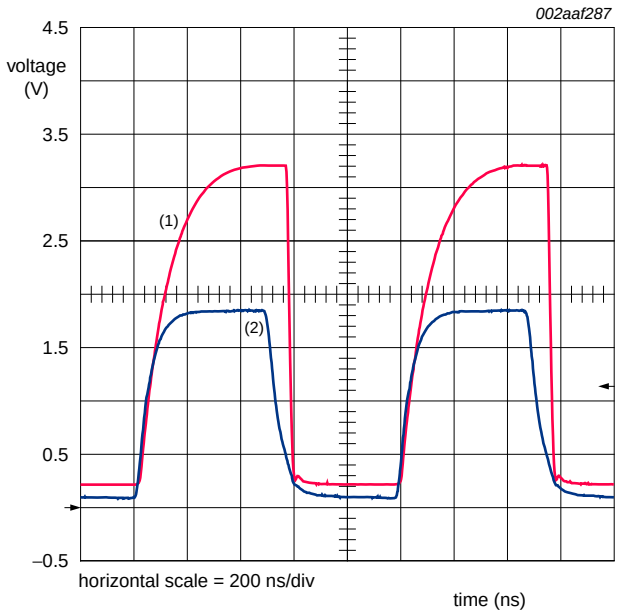
(2) Output 120 pF

Fig 9. Fall time (4 mA pull-up)

10. Application information

10.1 Design considerations

Figure 10 shows the PCA9521 level shifting signals from 1.8 V to 3.3 V at 1 MHz clock speed. The PCA9521 has excellent application to extending loads and providing interfaces to connectors on high speed microprocessor cards, well in excess of the Fast-mode 400 kHz I^2C-bus specification. Rise times are determined simply by the side of the buffer with the slowest RC time constant.



(1) Input 33 pF

(2) Output 120 pF

Fig 10. 1.8 V to 3.3 V level shifting at 1 MHz

Figure 11 shows a typical application for the PCA9521. The IC can level shift between different bus voltages without the need for external components. Higher bus voltages and currents outside the range of the Standard-mode I^2C-bus specification can be catered for, providing a longer range capability and higher noise immunity.

The enable pin (EN) can be used to interface buses of different operating frequencies. When certain bus sections are enabled, the system frequency may be limited by a bus section having a slave device specified only to 100 kHz. When that bus section is disabled, the slow slave is isolated and the remaining bus can be run at 400 kHz. The timing performance and current sinking capability will allow the PCA9521 to run well in excess of the 400 kHz maximum limit of the Fast-mode I^2C-bus.

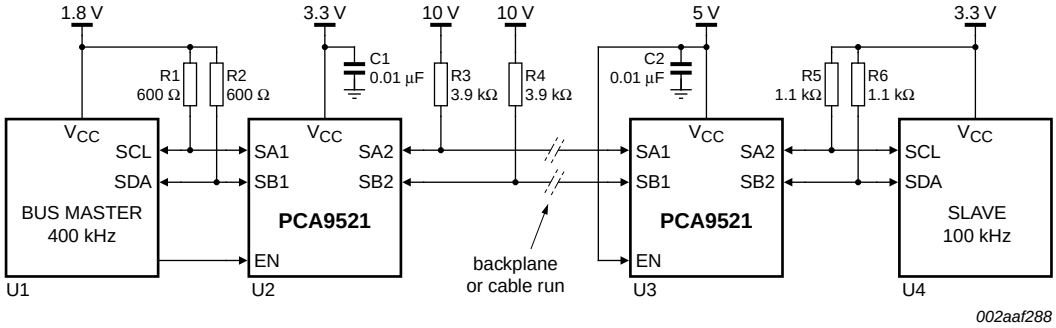
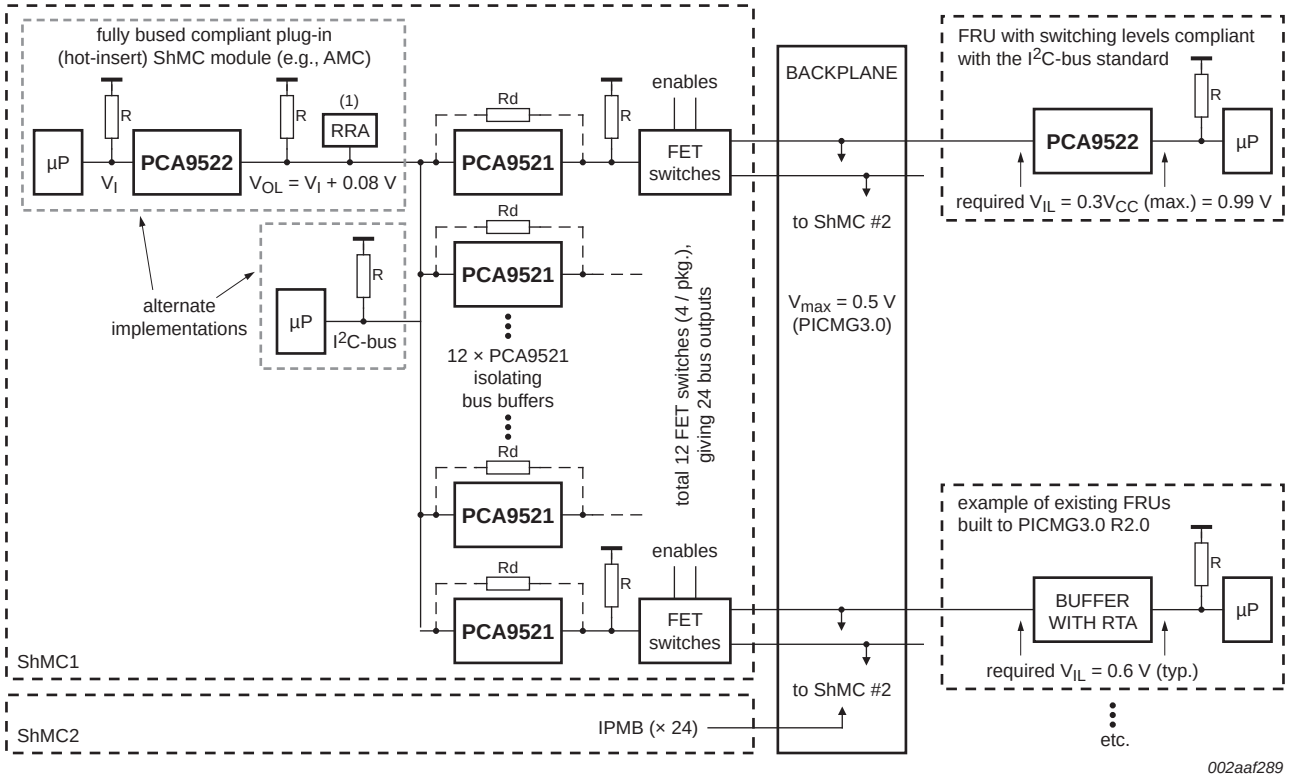


Fig 11. PCA9521 typical buffer application

Figure 12 shows the PCA9521 used in a radial (star) configuration on an AdvancedTCA Shelf Management Controller board (ShMC). The PCA9521 is highly suited to this and other backplane applications, providing excellent noise margins and I²C-bus compliant switching levels.



The system shown here uses FET switches, however a valid alternative is to simply use 24 × PCA9521's without FET switches.

Long track runs on the ShMC board and backplane can sometimes result in high frequency tuned circuits on either side of the PCA9521. If your layout is prone to forming such tuned circuits, it is perfectly acceptable to use a 'traditional' damping resistor (Rd) across the PCA9521.

(1) RRA = Rise Rate Accelerator.

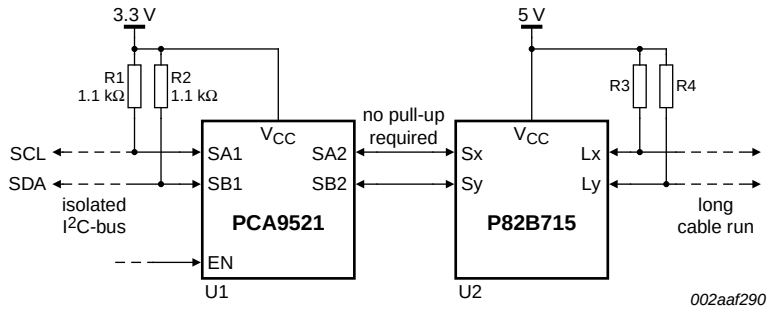
Fig 12. AdvancedTCA style backplane application using PCA9521 in a radial Shelf Manager configuration

Peripheral cards (or FRU (Field Replaceable Units)) and backplanes operating at a range of voltages can be interfaced together using a minimum of components. The PCA9521 can be teamed with the PCA9522 to achieve substantial noise margin gains across a system.

Multiplexers such as the PCA9544A are simple analog switches which provide no capacitive load isolation between connected branches. Figure 14 shows the PCA9521 enhancing an I^2C-bus multiplexer application, by isolating the load capacitance of each branch. Figure 15 and Figure 16 show alternate forms of bus multiplexing.

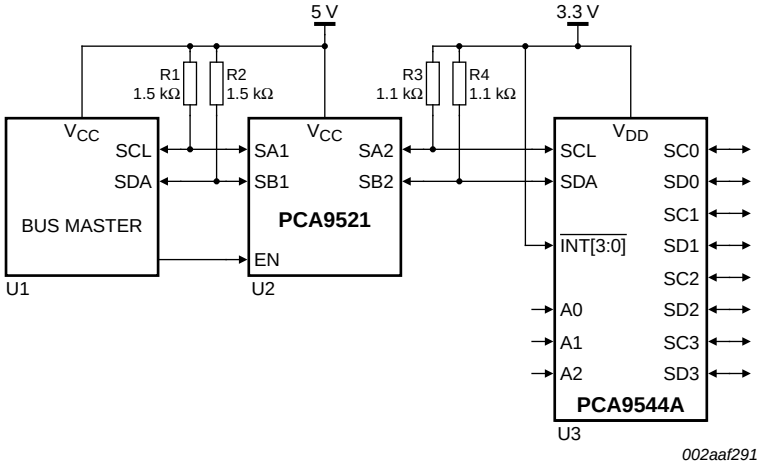
Similarly, the P82B715 I^2C-bus extender, which is commonly used for line driver applications, provides a '10× impedance transformation' but does not isolate either side of the buffer. Figure 13 shows the PCA9521 used to isolate the bus loading due to the P82B715. This greatly simplifies calculation of the pull-ups, increases the total system loading capability in extender applications, will meet the Fast-mode release requirement (when PCA9521 and P82B715 V_{CC}'s share a common supply), and ensures the 300 ns rise time requirement can easily be met even if the cable bus rise is relatively slow.

Buffers are intended to extend total system capacitance above 400 pF, so anticipate high capacitance on each side. When loading on one side is small, adding 47 pF is suggested to avoid any waveform ripple, should it occur.



PCA9521 provides bus isolation and simplifies calculation of bus RC components.

Fig 13. PCA9521 isolating the Standard-mode I^2C-bus from a P82B715 used as a line driver



Alternately, using the PCA9546A (which allows multiple outputs to be selected) you would simply place a PCA9521 on each output on the right-hand side, rather than a single PCA9521 on the left-hand side

Fig 14. PCA9521 multiplexer isolation application

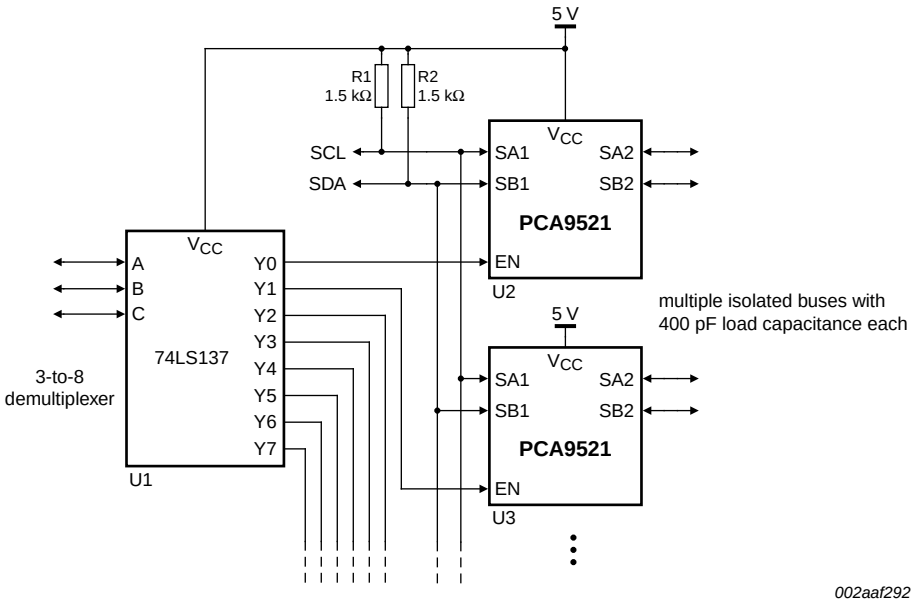


Fig 15. PCA9521 bus multiplexer application driven from a simple logic device

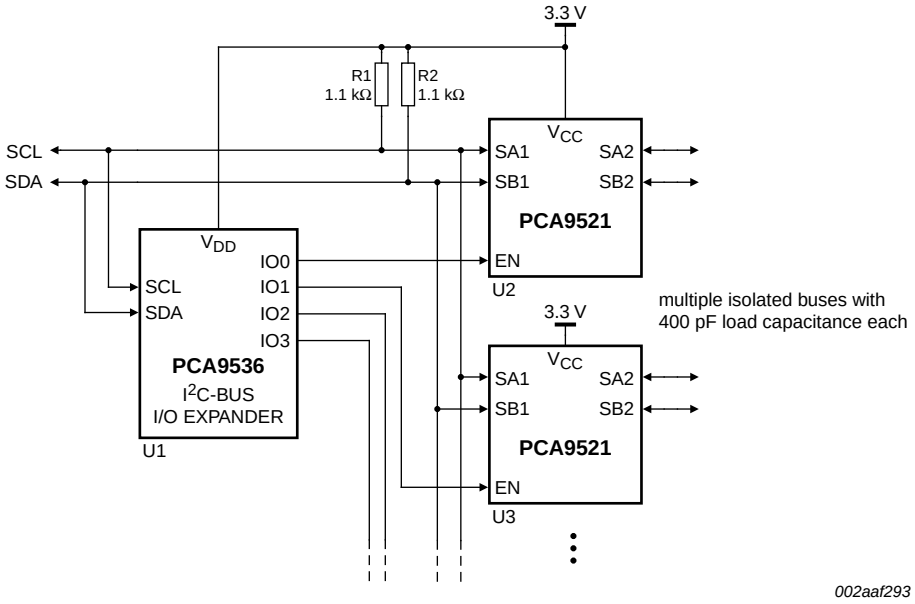


Fig 16. PCA9521 bus multiplexer application driven from an I²C-bus I/O expander

10.2 Input to output offset voltage calculation

The offset voltage between the side acting as the output (Sxx(out)) and the side acting as the input (Sxx(in)) of the PCA9521 can be calculated using the relationship given in Equation 1:

$$V_{offset} = V_i + 50\ mV + \left(\frac{V_{BUS}}{R}\right) \times 11 \quad (1)$$

This calculation is valid for $V_{bus(in)} \geq 200$ mV, as below this point the saturation voltage of the open-collector output drive transistor will begin to affect the characteristic. Input and output voltages are shown in millivolts, V_{BUS} (the supply voltage to the bus) is in volts, and R is in ohms.

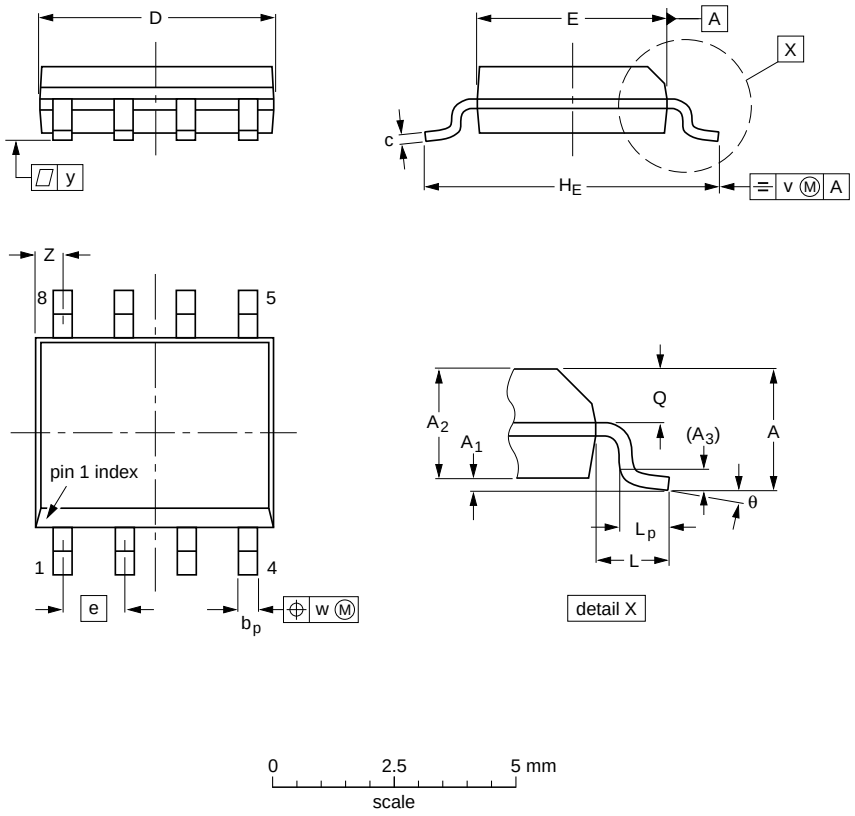
An example calculation for V_{BUS} = 3.3 V, V_{SA1} = 200 mV, the resistance R pulling up SA2 is 2 kΩ, then the voltage on SA2 is typically:

$$V_{SA2} = 200\ mV + 50\ mV + \left(\frac{3.3}{2000}\right) \times 11 = 268\ mV \quad (2)$$

This can be compared with the offset characteristic shown in Figure 5.

11. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

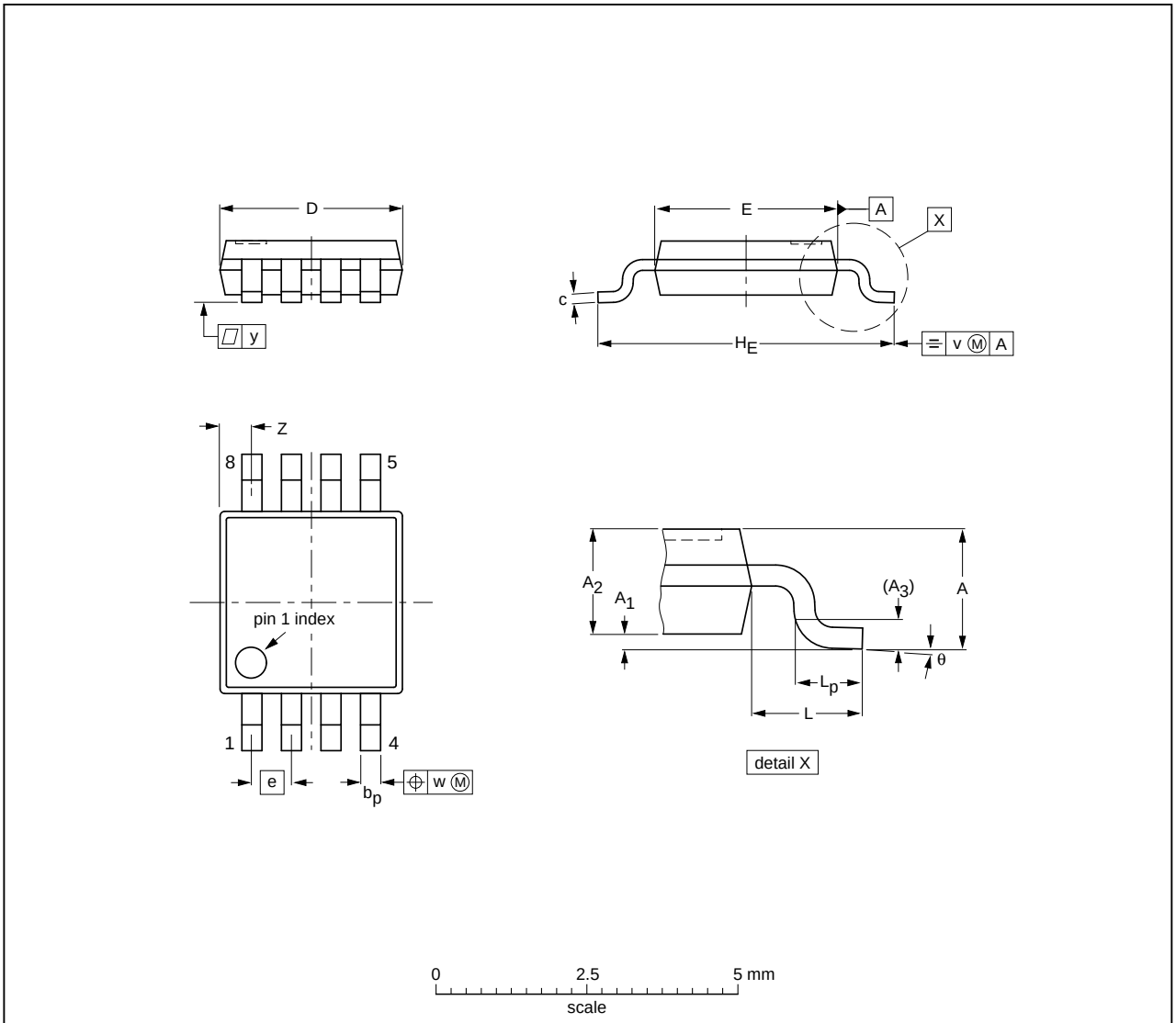
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 17. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 18. Package outline SOT505-1 (TSSOP8)

12. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 5 and 6

Table 5. SnPb eutectic process (from J-STD-020C)

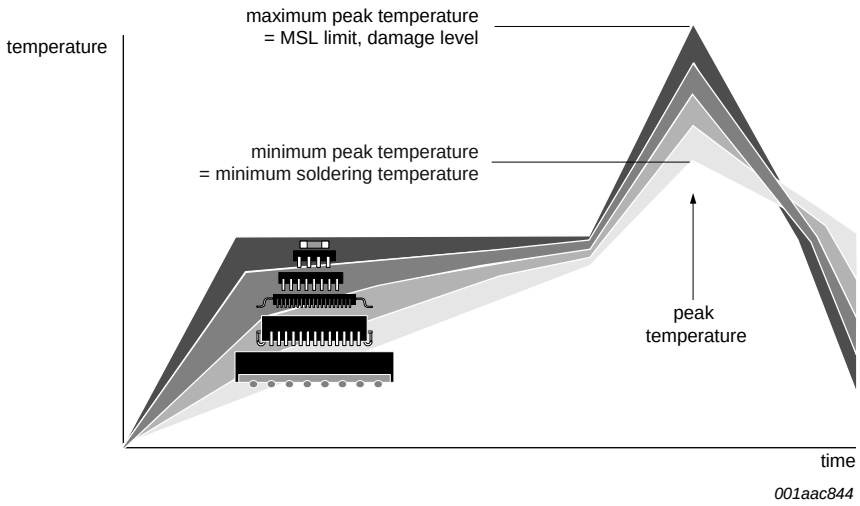
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 6. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.



MSL: Moisture Sensitivity Level

Fig 19. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 7. Abbreviations

Acronym	Description
ATCA	Advanced Telecommunications Computing Architecture
CDM	Charged-Device Model
cPCI	compact Peripheral Component Interconnect
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
IC	Integrated Circuit
IPMB	Intelligent Platform Management Bus
PICMG	PCI Industrial Computer Manufacturers Group
PMBus	Power Management Bus
RAID	Redundant Array of Independent Discs
SMBus	System Management Bus

15. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9521 v.1	20110822	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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